

A Shuttle Story: Latchup Qualification of a Truly Commercial Instrument

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Destructive single event effects (DSEE) are a main concern for pioneers attempting to use COTS (commercial-off-the-shelf) devices in space, so a COTS instrument full of such devices is particularly scary. We describe in this presentation the steps undertaken to understand and minimize the DSEE risks associated with flying several commercial electronic distance measurement units (EDMs or, sans jargon and acronyms, electronic rangefinders) for eleven days in a shuttle mission, known as SRTM (see Slide 2 and <http://southport.jpl.nasa.gov/html/projects/srtm.html> for more details on the mission). Although the cosmic ray ion and the trapped proton fluences for a short low earth non-polar orbit are quite low, there are COTS devices with large latchup cross sections and low LET thresholds to present a serious mission risk [1].

The EDM is a truly commercial, micro-controller-based instrument, densely packed with integrated circuits (see Slides 3 - 5). A proton latchup test of the whole instrument is fairly straightforward (Slides 6-8), requiring no delidding or parts identification. Simply irradiating all the parts to 10^9 protons ($200 \text{ MeV}/\text{cm}^2$) should be enough (almost three orders of magnitude above expected levels), and the instrument showed no DSEEs. However, (overly conservatively-?) irradiating to higher levels did reveal some operational difficulties: lockups, measurement slow downs, and the generation of error messages instead of distance measurements. These difficulties responded to commanded reset and/or to re-powering until, finally, while irradiating the micro-controller, an unrecoverable error occurred. Subsequently, the instrument was repaired by re-programming its serial EEPROM which apparently stores important system parameters.

Heavy ion considerations (see Slide 9) led us to conclude that even in the absence of proton latchup, there could still be a significant latchup risk. From Johnston et al. [1], the proton results probably give reasonable assurance of a heavy ion SEL threshold above $7 \text{ MeV per mg}/\text{cm}^2$. However, the project concluded they would be more comfortable with a clean "bill of health" for SEL to $\text{LET}=17$. To de-lid and test all the ICs represents a huge and costly effort, so identification of "tall tent poles" was done first.

At our request (and for a price), the manufacturer was able to come up with a parts list, although inspection of the first EDM sample (obtained to ascertain operational characteristics, and, subsequently subjected to "shake-and-bake") revealed several cases of substitution of parts from alternate manufacturers. Unfortunately, from a latchup standpoint, there's no such thing as a generic device. First, all CMOS ICs were identified (bipolar latchup is unlikely), and several were identified for replacement without testing: two op-amps and a 555 timer have bipolar equivalents (identical footprint) and a rad-hard pin-compatible SRAM (wider footprint, can be kludged in). Taking x-rays to determine die areas, we identified four large device types for heavy ion testing (see Slide 10) at an accelerator. Herculean (and lucky) efforts by one of the authors (O'Connor) yielded a working system with the four parts de-lidded. Unfortunately, the accelerator test was cut short when an unrecoverable error occurred as the first few ions hit the micro-controller. Like the proton test, subsequent (and proprietary) re-programming of the EEPROM restored instrument functionality.

Realizing that Californium-252 fragments give an effective LET of almost 17 for SEL, we were able to recover from the above fiasco by irradiating using one of JPL's Cf^{252} source. The four parts withstood more than 10^5 fragments/ cm^2 without exhibiting SEL. Subsequently, the EEPROM was delidded and also didn't latchup under Cf^{252} irradiation. Again, however, the micro-controller upset relatively easily into a disturbing and permanent large miscalibration; we concluded that, again, bad parameters had found their way into the EEPROM as the result of an upset.

In conclusion, a mixed approach of proton irradiation, part replacement, and heavy ion irradiation of selected devices provided a reasonable assurance of avoiding catastrophic DSEE for the EDM for the SRTM mission. Integration and operational changes are also being considered based on these test results: (1) turning the EDM off as much as possible and/or (2) providing the ability to re-load the EEPROM in flight. Finally, the test methodology of board level testing worked well, and, in the absence of SEL, even identified the most important upset consequences which the usual individual part testing would probably not have uncovered.

[1] A.H. Johnston et al., "Latchup in Integrated Circuits from Energetic Protons," *IEEE Trans. Nucl. Sci.*, V. 44, pp. 2367-2377, Dec. 1997.

[2] J. Levinson et al., "Single-Event Latchup (SEL) in IDT SRAMs- Dependence on Ion Penetration Depth," *Proc. 1993 RADECS Conf.*, pp. 438-440 (1993)

A Shuttle Story

Latchup Qualification of a Commercial Instrument

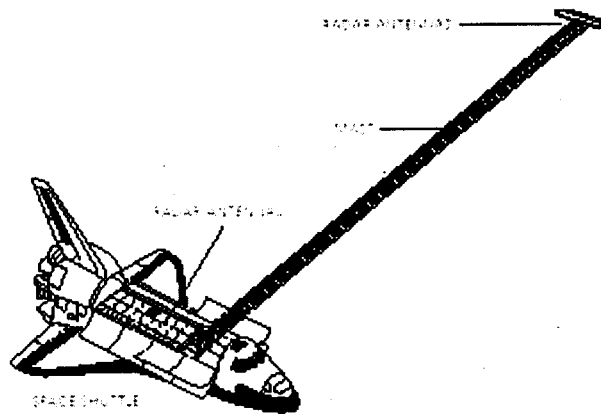
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(under contract with NASA)**

Summary

- **The Mission -- SRTM**
- **The Instrument -- EDM**
- **The Testing -- for Destructive SEE**
 - **Protons at IUCF**
 - **Heavy Ions at Texas A&M**
 - **Heavy Ions using JPL's Cf²⁵²**
- **The Results**

SRTM: Shuttle Radar Topography Mission



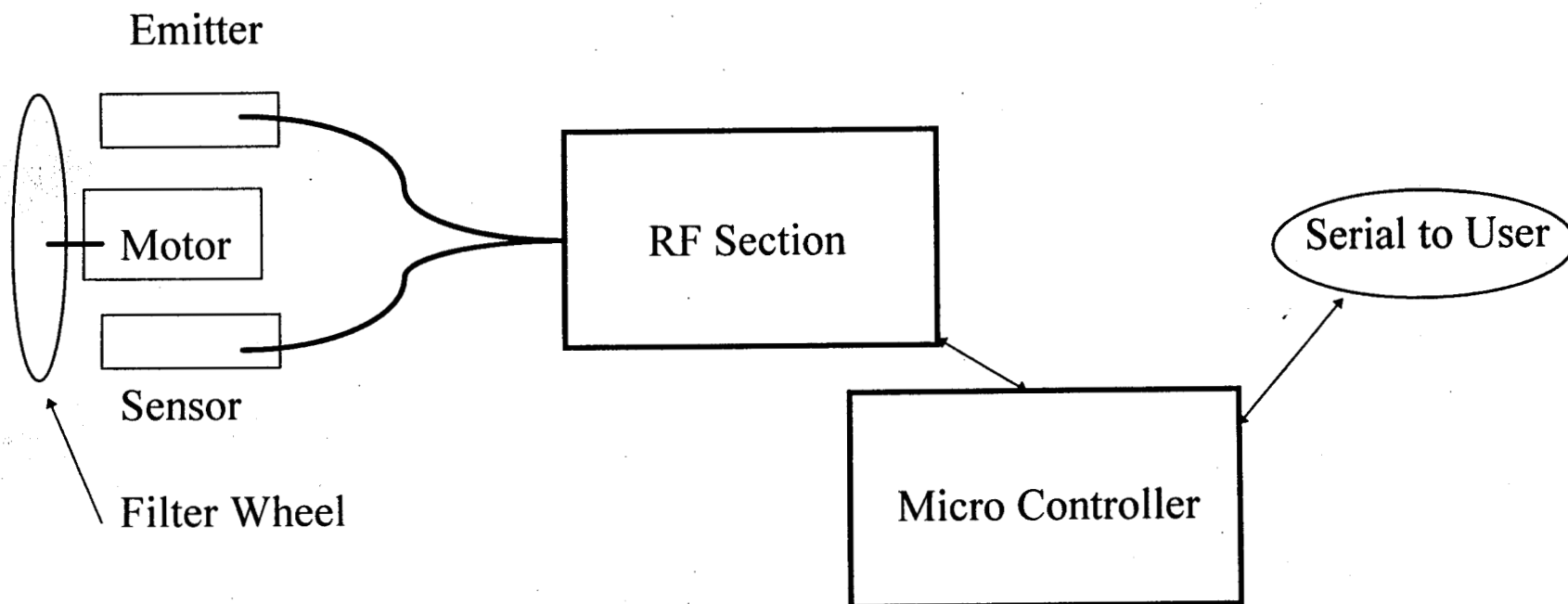
to make the “most accurate and complete topographic map of the Earth’s surface ever assembled”

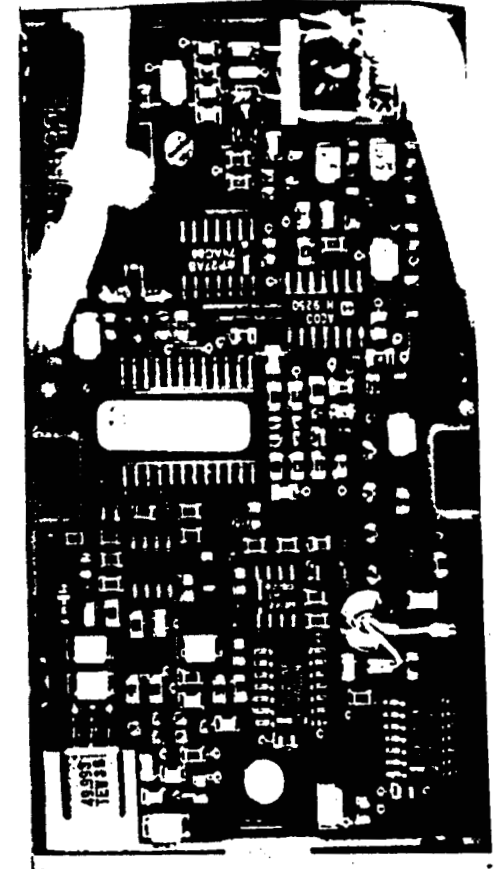
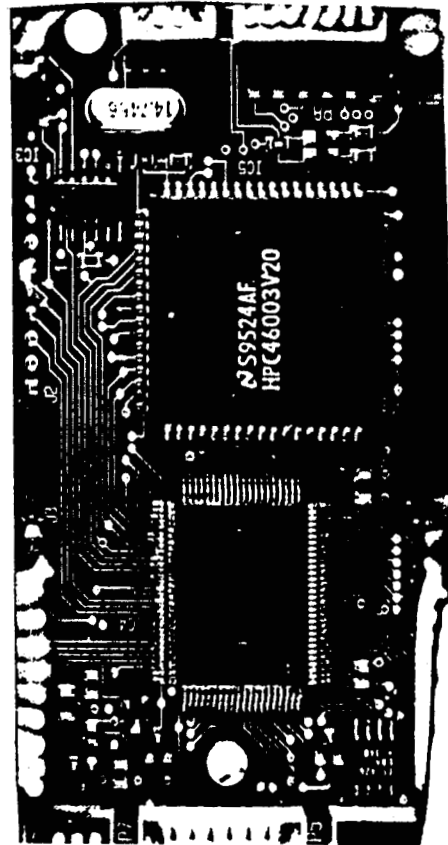
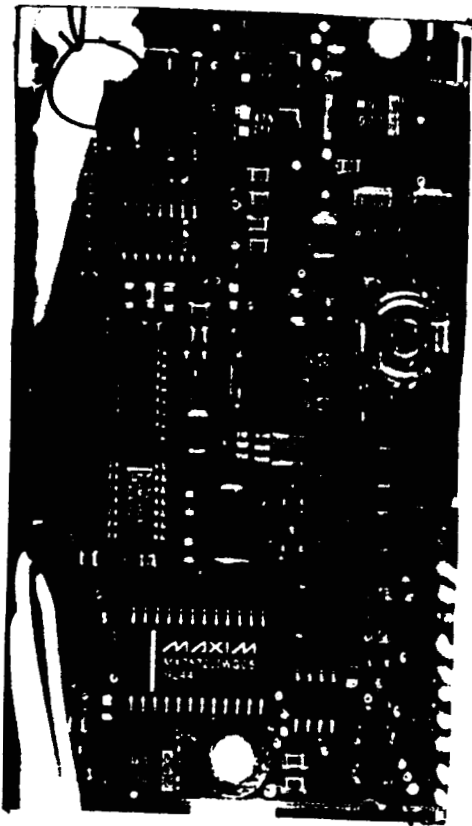
- **Eleven days at 233 km, 57 degrees**
- **Less than 10^6 protons**

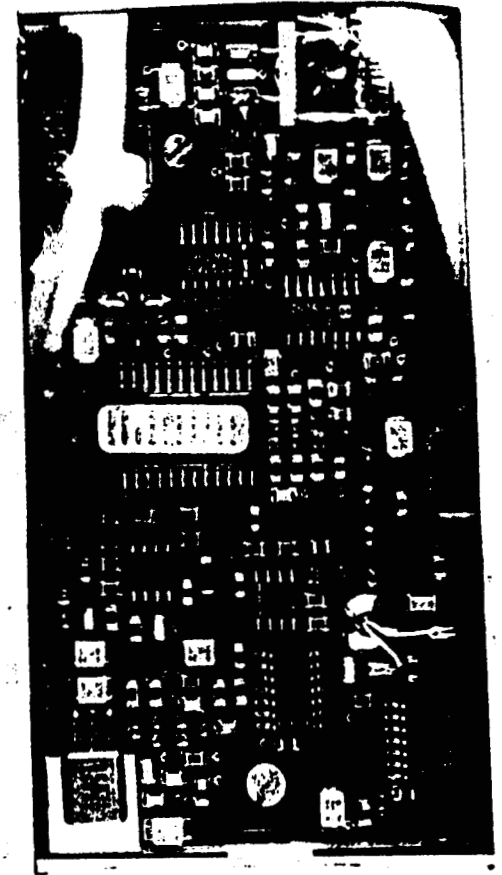
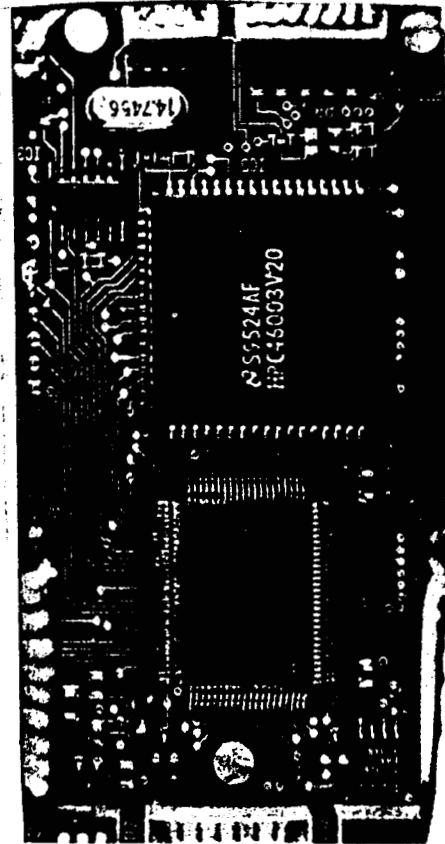
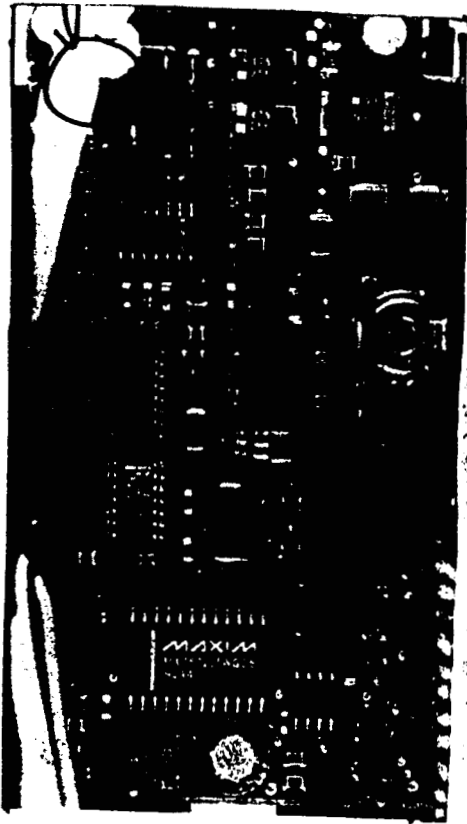
EDM: Electronic Distance Measurement (Rangefinder made by LEICA)

- **Three stacked boards in “butter” box**
- **30 IC’s, in surface mount plastic packages**
- **True COTS instrument**
 - **Parts list hard to get**
 - **Discrepancies between list and actual parts**
 - **No circuit diagram**
 - **No software source**

EDM Block Diagram







Latchup Testing

- **Monitor Functionality**
 - **Laptop and Printer**
 - **Continuous measure mode**
- **Monitor Current**
 - **Sub. programmable power supply for battery**
 - **Nominal currents:**
 - 11 mA on -12 V**
 - 297-302 mA on + 12 V**
 - **Shutdown on high current**

200 MeV Proton Testing

- **Irradiate six “half” boards (both sides at once)**
- **Increment through three fluence steps:**
 $10^9, 10^{10}, 10^{11} \text{ p/cm}^2$
- **Send EDM out for repair**

200 MeV Proton Test Results

- **Good News: No Single Event Latchup**
- **Bad News: Several types of SEEs**
 - **Measurement slow downs and lock ups**
 - **Error messages**
 - **RF section upsets at higher flux only**
- **Good News: SEEs temporary**
 - **Many affect only one measurement**
 - **Some respond to reset command**
 - **Rest cleared with power cycle** **EXCEPT**
- **Bad News: Last lock required “re-programming”**

GCR Heavy Ion Latchup for SRTM

Rates per cm² of susceptible chip area

Threshold LET	SEL Rate (100 mil Al)	SEL Rate (4000 mil Al)
1	14	13
3	2	2
5	0.8	0.7
10	0.2	0.2
17	0.01	0.01

Heavy Ion Test Preparation

- **X-rayed boards for die areas**
- **Identified five large suspects:**
 - μ P, SRAMs, PROMs, ASIC, and gate array**
- **And one small: EEPROM**
- **Decided to replace SRAMs (known problem)**
- **De-lidded other four large suspects**

Heavy Ion Testing at Cyclotron

- Chose LET=17 beam
- Irradiated processor first
- EDM failure occurred
with less than 3×10^3 ions/cm²
- Only one unit, so failure ended a very short test

Heavy Ion Testing with Californium

- **Fission fragments give LET=17 for latchup ??**
(from some test evidence and Johnston model)
- **Irradiating processor last --**
other three show no SEL to 10^5 ions/cm²
processor caused two quick failures,
including a permanent miscalibration
but no SEL

Additional Steps

- **Will replace SRAMs with rad-hard (SEU-hard)
pin compatible (not footprint compatible)**
- **Irradiated EEPROM with Cf²⁵², no SEL**
- **Considering low “on” duty cycle**
- **Replacing CMOS op-amps and timer with
footprint compatible bipolar equivalent**

Conclusions

- **Board / system level testing IS worthwhile when part level testing is not feasible**
- **Without the system level test, we would have missed the most likely on-orbit SEE effect:**
processor upsets corrupting important parameters stored in non-volatile memory
- **Proton testing by itself is not enough, even for a shuttle mission**